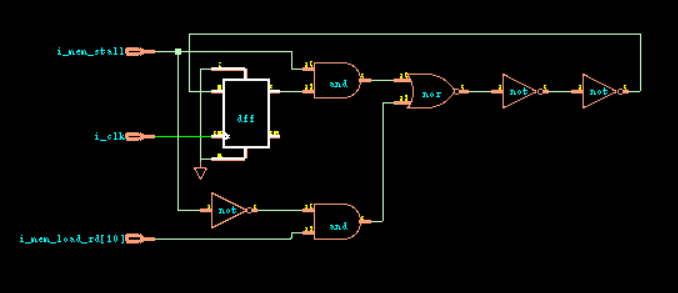
Part A

1.A brief report describing the netlist bugs and your resolution.

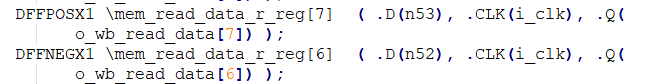
There are three netlist bugs:

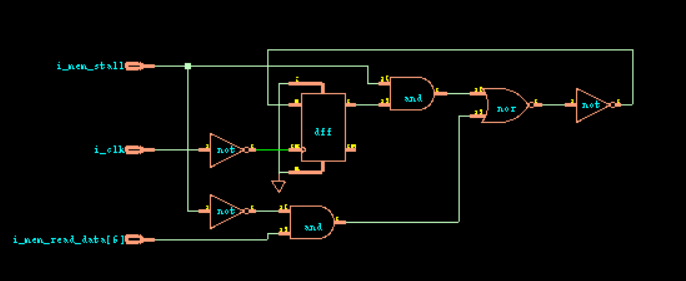
The first one is causing a duplicated inverter.



Solution: I delete the INVX1 U930 and reconnect the wire as INVX1 U93(.A(n91),.Y(n880)),

The second one is





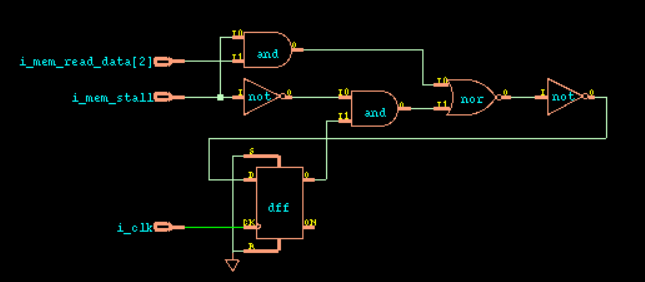
It should use a positive DFF as reg[7].

Solution: I correct the negative to positive as DFFPOSX1…

The third one is

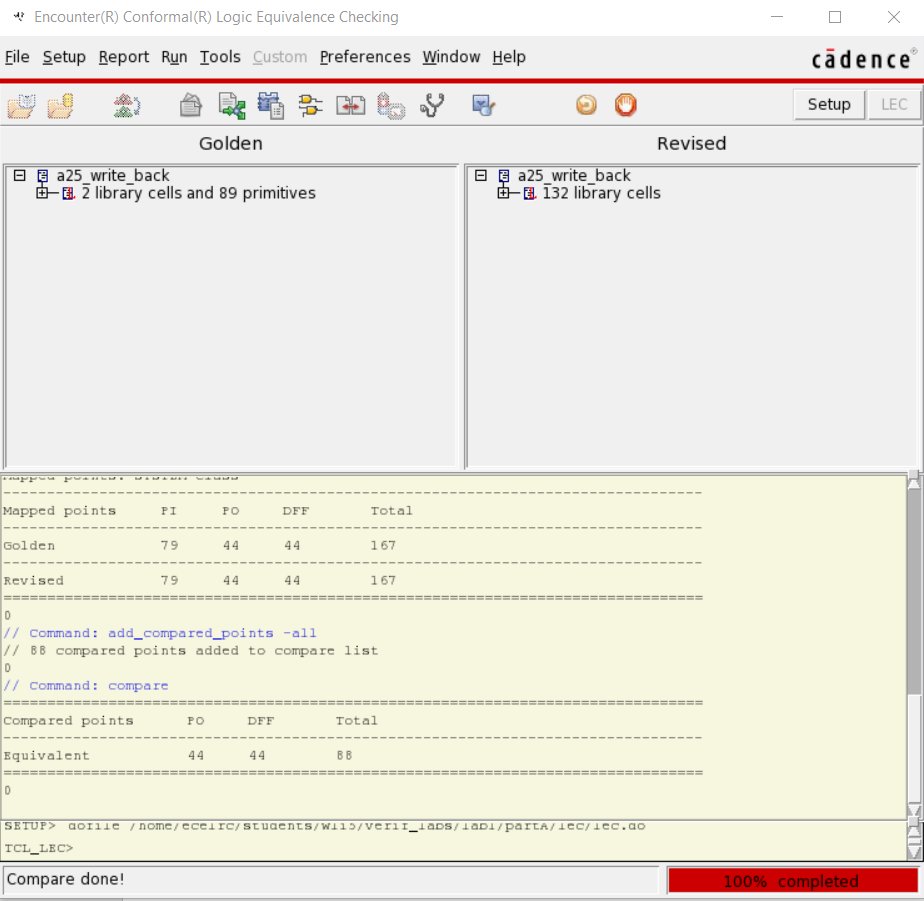


The MUX2x1 U174 is wrong. The input wire is reversed.

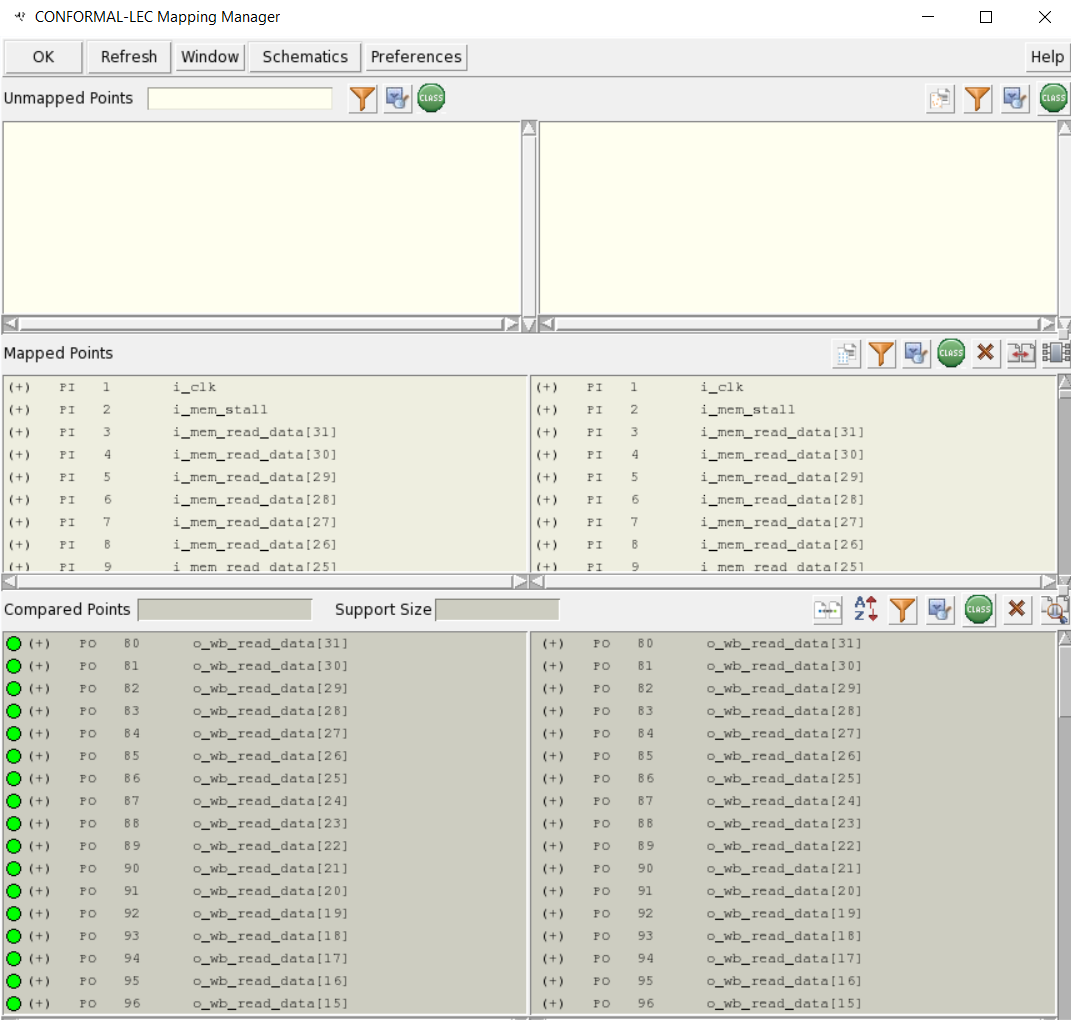


Solution: I change the order of .B and .A as MUX2X1 U174 ( .B(i\_mem\_read\_data[2]), .A(o\_wb\_read\_data[2]), .S(i\_mem\_stall), .Y(n131) );

2.Lec Console:



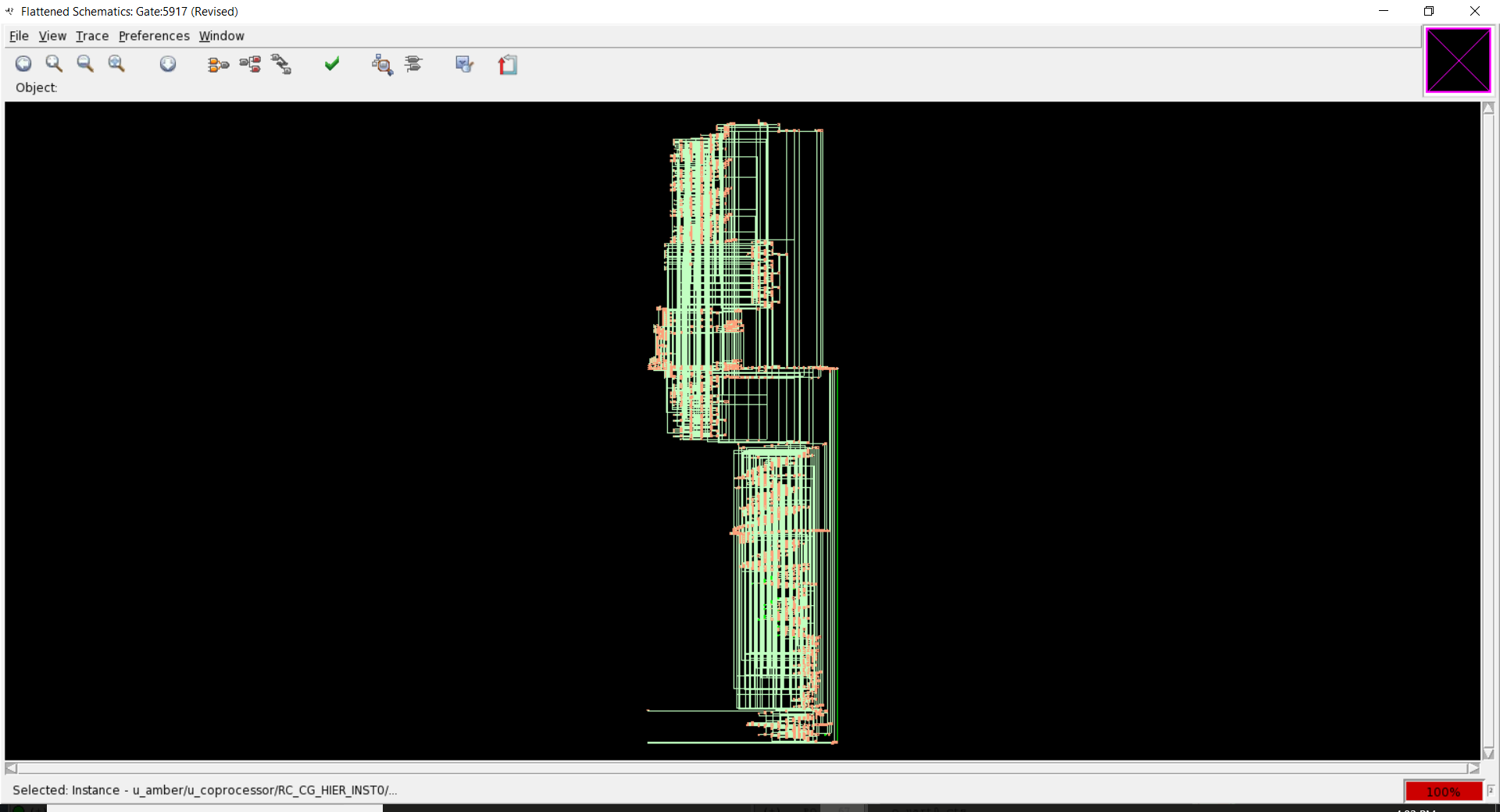
Mapping manager:

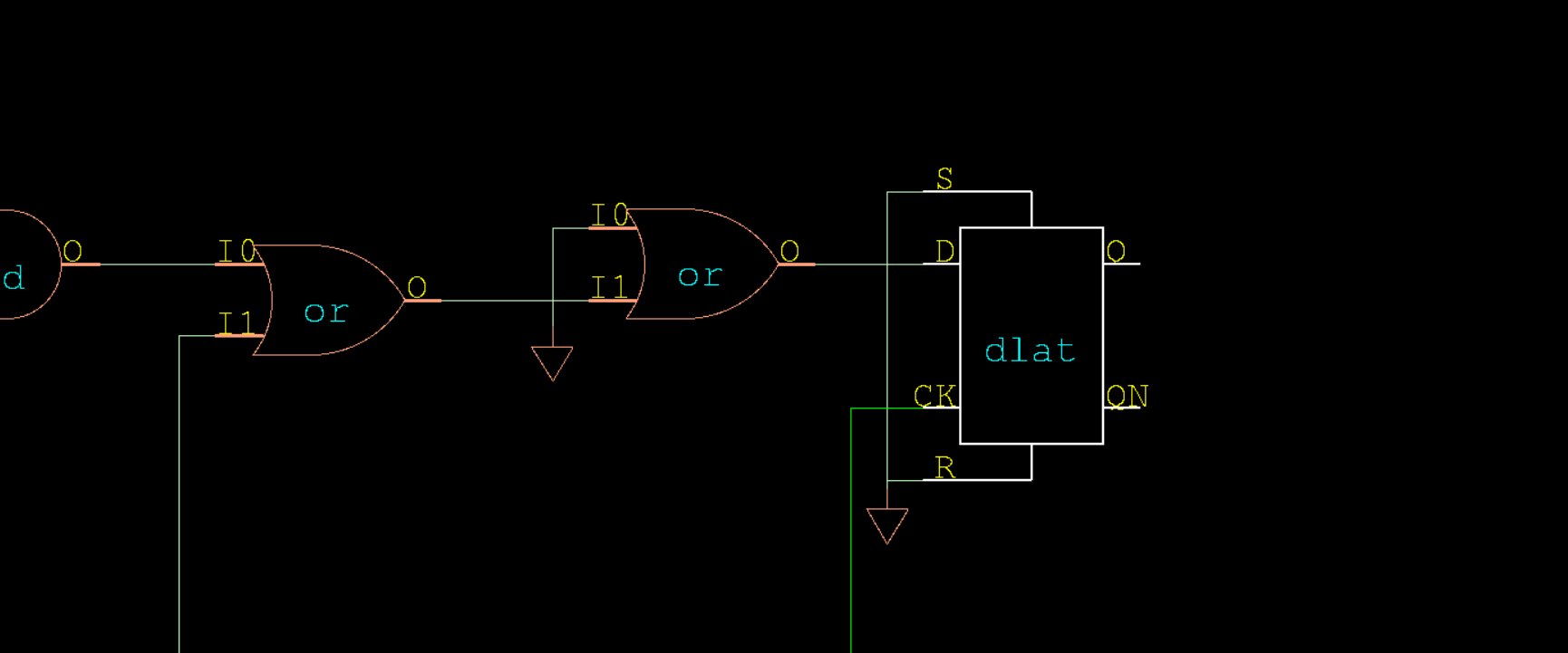


PartB:

1.The scan style is muxed\_scan which includes scan insertion and clock gating. Since they are not present in the RTL, so I have to add constraints to disable the clock gate and the added scan logic. And in the test signal objects, since they are all in high active, I set the constraint to 0 to disable the scan.

2.





3. set\_flatten\_model -seq\_constant -seq\_constant\_x\_to 0

Remodel registers that also have feedback to constants.

Optimize the flip-flop to a constant zero when the flop is always in a don’t care (x) state.

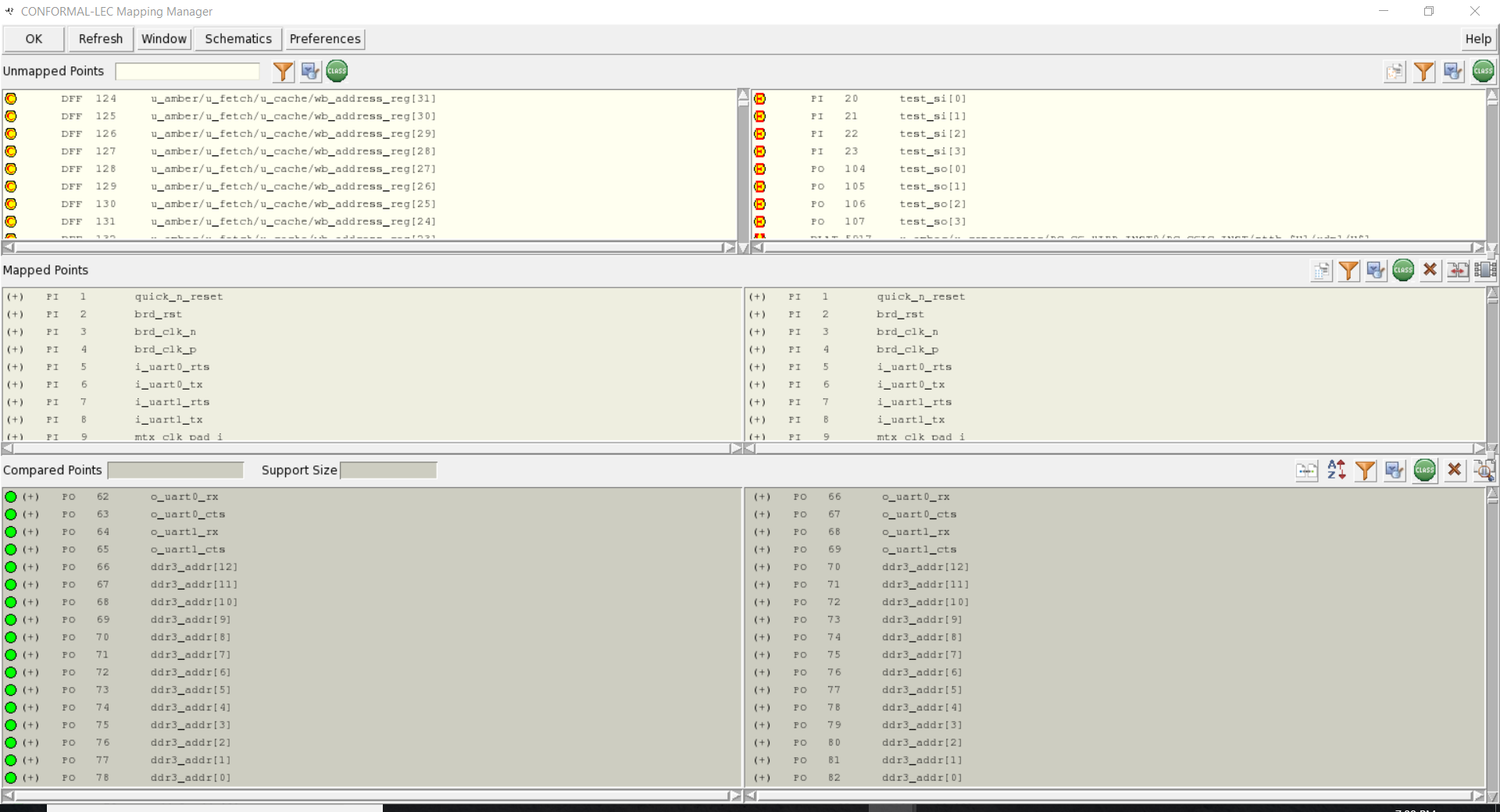
set\_flatten\_model -gated\_clock

Remodels the gated-clock logic of the clock port of a DFF.

set\_analyze\_option -auto

Determine the best place to run the ANALYZE SETUP command. Enable the automatic analysis.

4.mapping manager



Lec console

